Alinteri J. of Agr. Sci. (2021) 36(1): 635-641
e-ISSN: 2587-2249
info@alinteridergisi.com

http://dergipark.gov.tr/alinterizbd
http://www.alinteridergisi.com/
DOI:10.47059/alinteri/V36I1/AJAS21090

RESEARCH ARTICLE

Construction of pMos Logic based Low Power High Speed Comparator Compare with nMos Logic

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ARTICLE INFO

Article History:
Received: 10.04.2021
Accepted: 17.05.2021
Available Online: 28.06.2021

Keywords:
Innovative pMos Logic based Comparator
nMos Logic based Comparator
Tanner Tool
Power Consumption
Green Energy

ABSTRACT

Aim: The aim of this work is to construct an innovative pMos logic based comparator and analyze the power consumption and compare with the nMos logic based comparator. **Material and methods:** The comparator is designed by using the Tanner tool version 16.01 for simulation and verification. By varying the length of a transistors in a circuit the power values were obtained. This experiment is performed for 20 different values of length. **Results:** The power consumption of a pMos logic based comparator was minimum (2.2656 ± 0.37933), followed by the nMos logic based comparator (7.7494 ± 0.41603), the less power consumption seen in pMos logic based comparator significance (.955). **Conclusion:** The consumption of power by the constructed pMos logic based comparator appears to have less power consumption than the nMos logic based comparator.

Please cite this paper as follows:

Devendra Reddy, M. and Dass, P. (2021). Construction of pMos Logic based Low Power High Speed Comparator Compare with nMos Logic. *Alinteri Journal of Agriculture Sciences, 36*(1): 635-641. doi: 10.47059/alinteri/V36I1/AJAS21090

Introduction

This method is about to design and analyse the power consumption of pMos logic based comparator and compare with nMos logic based comparator (P. Dass 2020). Today, the necessity of ultra-low power, high speed and efficient devices like ADC leads to the use of comparators to make rapid decisions (Kumar and Kumar 2016). Analog-to-Digital converters convert analogue quantities into the digital language that is used in information processing, computing, transmission, and control systems. So, digitised signals are used in almost every application. ((Varshney and Nagaria 2020). The output of high velocity analogue to digital converters is essentially determined by the comparator. Low-power and high-speed ADCs are critical building blocks in the front-end of a radio-frequency receiver in most modern telecommunication systems (Sarfraz Hussain, Kumar, and Trivedi 2017).

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Due to their important role in modern communications, speed and power consumption in mobile equipment, analogous to digital converters, were more attracted(Razavi, Tavakoli, and Setoudeh 2020).

The total number of articles published in this topic over the past five years are more than 200. A low power consumption and high speed. Gate Diffusion Input (GDI) is one technique of low energy efficiency and area efficiency. GDI's disadvantage is its low logic output swing(Swetha 2016). An XNOR port using three transistors with a power consumption analysis with eight transistors using CADENCE EDA 90nm technology (Manikannan, Mahendran, and Prabakaran 2017). A novel modified comparator is a combination of adiabatic logic 2N-2N2P and two static adiabatic clocked logic (2N-2N2P and PASCAL), efficient charge recovery logic adiabatic and two phases static adiabatic static clocked logic (ECRL and 2PASCL)(T. S. A. Samuel et al. 2017). The offset is suppressed by dynamically storing the comparator offset on the input capacitors(Liu et al. 2017). Adiabatic logic is used to produce a 1-bit adder for low power consumption (Saladi and Leela

Kumari 2021). A pair of hybrid 1-bit complete adder cells that use both pass transistor and transmission gate logic and are low-power and high speed (Tirumalasetty and Machupalli 2019). The best overall work is low power consumption and high speed. Gate Diffusion Input (GDI) is one technique of low energy efficiency and area efficiency. GDI's disadvantage is its low logic output swing(Swetha 2016).

Previously our team has a rich experience in working on various research projects across multiple disciplines (Sathish and Karthick 2020; Varghese, Ramesh, and Veeraiyan 2019; S. R. Samuel, Acharya, and Rao 2020; Venu, Raju, and Subramani 2019; M. S. Samuel et al. 2019; Venu, Subramani, and Raju 2019; Mehta et al. 2019; Sharma et al. 2019; Malli Sureshbabu et al. 2019; Krishnaswamy et al. 2020; Muthukrishnan et al. 2020; Gheena and Ezhilarasan 2019; Vignesh et al. 2019; Ke et al. 2019; Vijayakumar Jain et al. 2019; Jose, Ajitha, and Subbaiyan 2020). Now the growing trend in this area motivated us to pursue this project.

The power consumption was analysed in the nMos logic based comparators but not in the pMos logic based comparators. So, The power consumption was analysed in pMos logic based comparator by varying the length of a transistors. Construction of low power digital comparator in pseudo nmos logic to reduce the power dissipation(P. Dass 2020).The aim of this study is to construct a pMos logic based comparator and analyze the power consumption and compare with the nMos logic based comparator.

Materials and Methods

The proposed work is to analyse the power consumption of pmos logic based comparator. The study is done in the Department of ECE, Saveetha School of Engineering and this work is not done by using the human samples. The total no of groups used in this project is 2. Group 1 is the pmos comparator (Experimental group) and group 2 is the nmos comparator (Control group). 20 samples were taken for the analysis of power consumed by the constructed comparator with the g power of 80%(Vijay et al. 2017).

The comparator was designed using the Tanner tool for simulation and verification. pMos logic is a family of digital circuits based on p-channel, enhancement mode metal-oxide-semiconductor field effect transistor. 20 different values of length of transistor were taken for the analysis. Same values of length were taken for both the groups (S. Hussain, Kumar, and Trivedi 2021).

In the existing system, N-type metal-oxide-semiconductor logic uses n-type MOSFETs to implement logic gates and other digital circuits. These nMOS transistors operate by creating an inversion layer in a p-type transistor body. The n-channel is created by applying voltage to the third terminal, called the gate (Vijay et al. 2017). In this comparator, 20 different values of length and width and analysis of power consumption was done. The design setup is simulated as a standard protocol (Shashank Shekhar 2015).

The power consumption values of designed and existing models for different values of length of transistors in a comparator as given in table 1.

Table 1. The power consumption values of designed and existing models for different values of length of transistors in a comparator.

Length(nm)	Power consumption of pMos comparator (milliwatts)	Power consumption of nMos comparator (milliwatts)
90	1.393	8.771
100	1.592	8.287
120	1.789	7.738
150	1.982	7.149
180	2.011	8.596
200	2.058	7.289
220	2.109	7.299
250	2.183	7.538
280	2.254	7.43
300	2.299	7.532
320	2.342	7.574
350	2.404	7.63
380	2.462	7.622
400	2.5	7.834
420	2.535	7.675
450	2.587	7.685
480	2.636	8.033
500	2.688	7.616
520	2.699	7.652
580	2.788	8.039

The SPSS version 2.1 Statistical software is used to compare the power values of pMos logic based comparator with the nMos logic based comparator. Descriptive statistics (mean, standard deviation, and standard error) were carried out for each model. This will give the mean, standard deviation, and standard error of the comparators. The independent variables in this study are Voltage source, length, width. The dependent variable is power. The analysis done on this work was the power consumption of a pMos logic based comparator compared with nMos logic comparator.

Results

Fig.1: it shows that the pMos logic based Comparator design in the S-Edit in tanner tool and simulation is done. Here, the 5 pMos transistors and 6 nMos transistors are used. When input is low the pMos transistors will work and simulate the comparator. Fig.2 it showed the power consumption of a pMos logic based comparator which is designed in a tanner tool at 90nm length of a transistors in a comparator. The power consumption in the designed comparator is low when compared with the existing models.

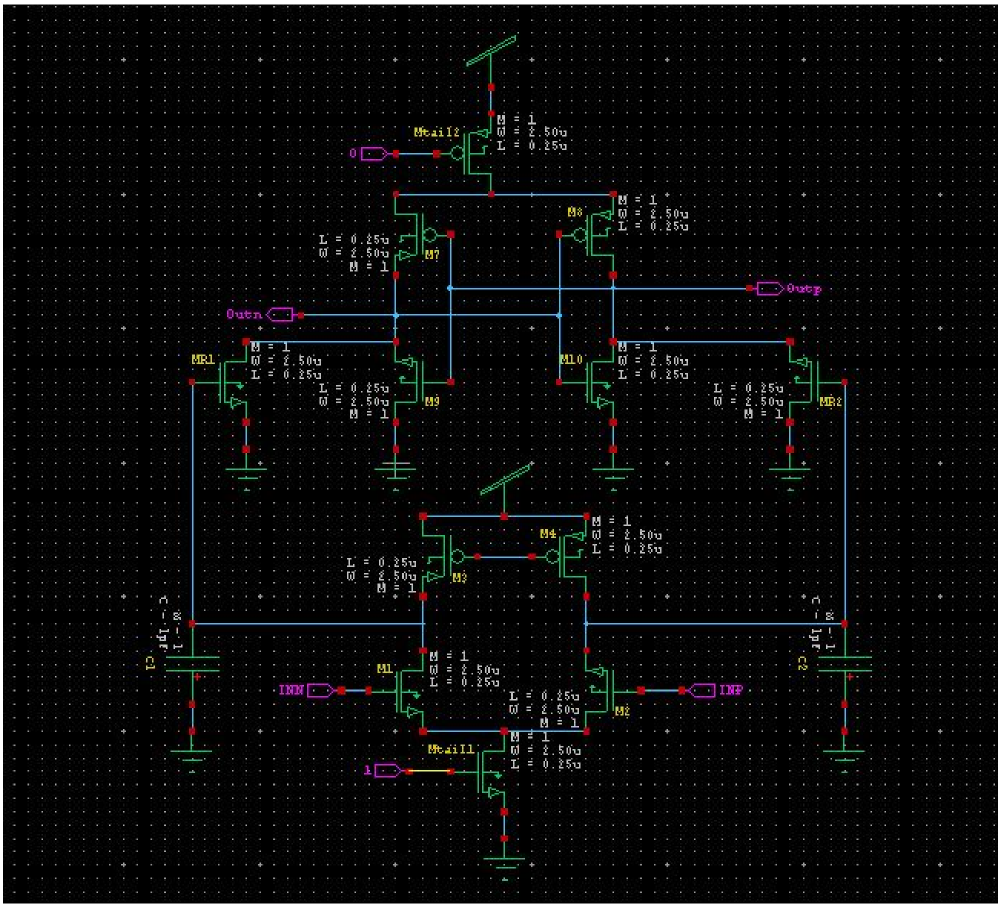

Fig.1. Represents the schematic diagram of a Pmos logic-based comparator

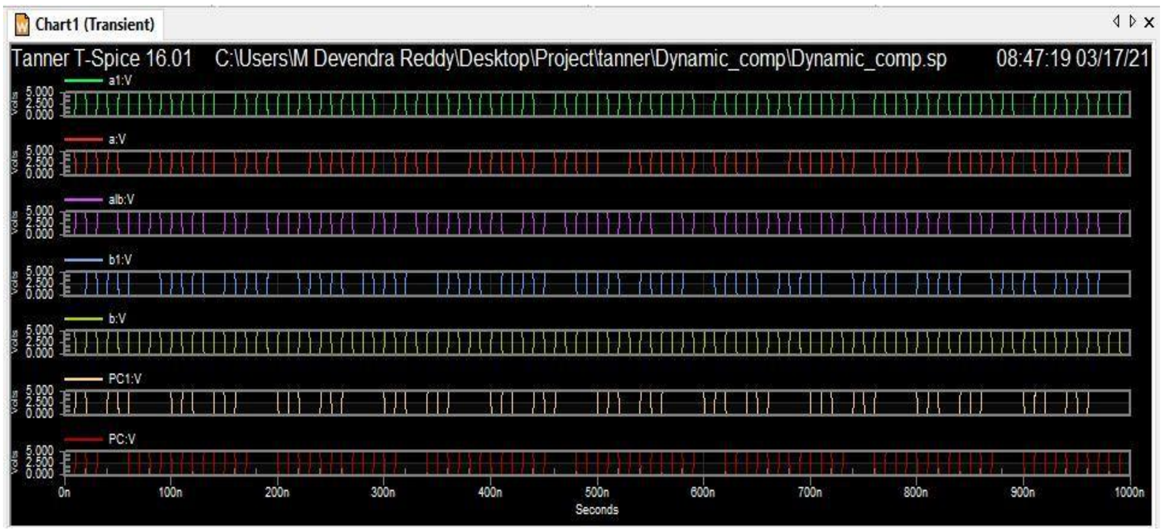

Fig.2. Represents the graph shows the power consumption of a pMos logic based comparator

In performing statistical analysis of 20 samples, pMos comparator obtained 0.38 standard deviation with 0.08 standard error while nMos comparator obtained 0.42 standard deviation with 0.09 standard error (Table 2). The standard deviation in Pmos comparator is low.

Table 2. shows the Mean, standard deviation, standard errors of the power consumption of a pMos logic comparator and nmos logic comparator independent sample t test was performed

Group	Mean	N	Std.Deviation	Std.Error Mean
pMos	2.2656	20	0.37933	0.08482
nMos	7.7494	20	0.41603	0.09303

Table.3: it shows that the mean standard deviation and significance difference of power consumption. The significant difference was observed between the group(p=0.955) from the independent sample test.

Table 3. Shows that the mean standard deviation and significance difference of power consumption. The significant difference was observed between the group(p=0.955) from the independent sample test

	Levene's Test for Equality of Variances		t-test for Equality of Means						
	F	sig	t	df	Sig. (2-tailed)	Mean Difference	Std. Error Difference	95% Confidence... Lower	95% Confidence Interval of the... Upper
Equal variances assumed	.003	.955	-43.561	38	.000	-5.48390	.12589	-5.73875	-5.22905
Equal variances not assumed			-43.561	37.681	.000	-5.48390	.12589	-5.73882	-5.22898

Figure.3: represents the comparison of power consumption of pMos logic based comparator and the nMos logic based comparator. It shows the power consumption of pMos logic based comparator is less and nMos logic based comparator is more. The mean power of pMos comparator is better than the nMos comparator.

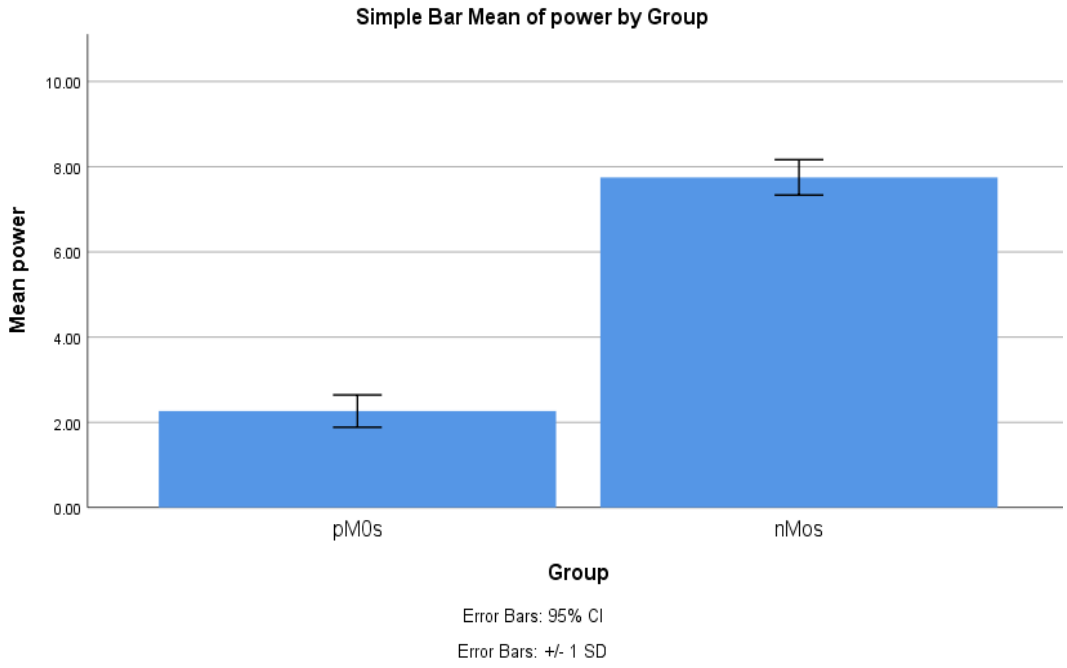

Fig.3. Comparison of pMos logic based comparator and nMos logic based comparator in terms of power. The mean power of the pMos comparator is better than the nMos comparator. pMos comparator vs nMos comparator Y Axis:- Mean power of detection ± 1 SD.

Discussions

In this method, the power consumption of pMos logic based comparator appears to consume less power compared with the nMos logic based comparator. We observed that the statistically insignificant and value obtained is 0.955.

The analysis of power consumption of pMos logic based comparator by varying the length of a transistors was done. At the input of the compare preamplifier and the latch stage, pMOS transistors are used. A special, local clock generator controls both phases. The lock is activated at the evaluation stage in time to achieve sufficient preamplification and prevent excess power consumption(Khorami and Sharifkhani 2018). At the first and second phases of the comparator input, PMOS transistors are used. The second phase is enabled in a pre-amplifier gain in the evaluation phase following the first phase by a predefined delay. In addition, following the delay, the first stage is shut down to reduce overall energy consumption (Khorami, Dastjerdi, and Ahmadi 2016).

Our institution is passionate about high quality evidence based research and has excelled in various fields ((Vijayashree Priyadharsini 2019; Ezhilarasan, Apoorva, and Ashok Vardhan 2019; Ramesh et al. 2018; Mathew et al. 2020; Sridharan et al. 2019; Pc, Marimuthu, and Devadoss 2018;

Ramadurai et al. 2019). We hope this study adds to this rich legacy.

Delay analysis of the low voltage dynamic comparator body-driven p-channel metal oxide semiconductor(Vijay et al. 2017).To achieve low electricity consumption by their mechanisms which modify circuit operation. The techniques are pseudo NMOS, CVSL, and power gating. Cascode Voltage Switch Logic. Renewable comparator at 90 nm CMOS with a supply voltage of 0.7 V is initially simulated(Khatak, Kumar, and Dhull 2018). For high speed applications with low power supply voltage, a new structure of the dynamic latch comparator is proposed. Each inverter contains a condenser which disconnects PMOS and NMOS gates(Ni et al. 2018). In our study, the tanner tool is used to simulate which is the best tool to design the comparators and calculate the power values. In this work, the power consumption as literature has reported less consumption in pMos logic comparator when compared with nMos logic comparator(P. Dass 2020). By varying the lengths of transistors in a comparator influence negatively. Here, the pMos transistor is used in design for reducing the power consumption. In the future we can use CMOS transistors to reduce power consumption.

Conclusion

By varying the difference length of transistors the pMos logic based comparator consumes less power. Thus, the results appear that the pMos logic-based comparator provides significantly less power consumption than the nmos logic-based comparator.

Declarations

Conflict of Interests

No conflict of interest in this manuscript.

Authors Contributions

Author MDR was involved in simulation and data analysis, manuscript writing. Author PD was involved in conceptualization, data validation, and critical review of manuscript.

Acknowledgement

The authors would like to express their gratitude towards Saveetha School of engineering, Saveetha Institute of Medical and Technical Sciences (Formerly known as Saveetha University) for providing the necessary infrastructure to carry out this work successfully.

Funding

We thank the following organizations for providing financial support that enabled us to complete the study.

1. Vee Eee Technologies Solution Pvt. Ltd., Chennai.
2. Saveetha University
3. Saveetha Institute of Medical and Technical Sciences.
4. Saveetha School of Engineering.

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